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Amdahl's Law

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Governs theoretical speedup

$$S = \frac{1}{(1-P) + \frac{P}{S_{parallel}}} = \frac{1}{(1-P) + \frac{P}{N}}$$

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P: parallelizable portion of the program

S: speedup

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Amdahl's Law

N: number of parallel processors

Amdahl's Law

Governs theoretical speedup

$$S = \frac{1}{(1-P) + \frac{P}{S_{parallel}}} = \frac{1}{(1-P) + \frac{P}{N}}$$

P: parallelizable portion of the program S: speedup

N: number of parallel processors

P determines theoretically achievable speedup

• example (assuming infinite N): $P=90\% \rightarrow S=10$ $P=99\% \rightarrow S=100$

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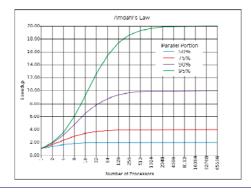
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How many processors to use

- when P is small \rightarrow a small number of processors will do
- when P is large (embarrassingly parallel) \rightarrow high N is useful



Focus Efforts on Most Beneficial SPIE Medic

Optimize program portion with most 'bang for the buck'

- look at each program component
- don't be ambitious in the wrong place

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Focus Efforts on Most Beneficial

Optimize program portion with most 'bang for the buck'

- look at each program component
- don't be ambitious in the wrong place

Example:

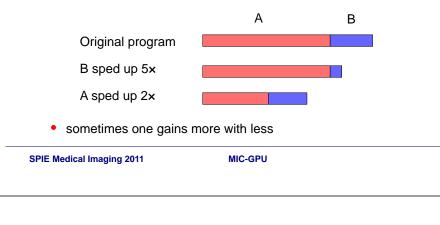
• program with 2 independent parts: A, B (execution time shown)

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Beyond Theory....

Limits from mismatch of parallel program and parallel platform

• man-made 'laws' subject to change with new architectures

Memory access patterns

· data access locality and strides vs. memory banks

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· data access locality and strides vs. memory banks

Memory access efficiency

· arithmetic intensity vs. cache sizes and hierarchies

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Beyond Theory....



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• data access locality and strides vs. memory banks

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• arithmetic intensity vs. cache sizes and hierarchies

Enabled granularity of program parallelism

• MIMD vs. SIMD

Beyond Theory....

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Enabled granularity of program parallelism

MIMD vs. SIMD

Hardware support for specific tasks \rightarrow on-chip ASICS

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Beyond Theory	SPIE Medical Imaging	Device Transfer Costs	SPIE Medical Imaging
Limits from mismatch of parallel program and parallel platform man-made 'laws' subject to change with new architectures Memory access patterns data access locality and strides vs. memory banks 		 Transferring the data to the device is also important computational benefit of a transfer plays a large role transfer costs are (or can be) significant 	
 Memory access efficiency arithmetic intensity vs. cache sizes and 			
Enabled granularity of program paralleMIMD vs. SIMD	lism		
Hardware support for specific tasks \rightarrow	on-chip ASICS		
Support for hardware access \rightarrow drivers	s, APIs		
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Device Transfer Costs



Transferring the data to the device is also important

- computational benefit of a transfer plays a large role
- transfer costs are (or can be) significant

Adding two (*N*×*N*) matrices:

- transfer back and from device: 3 N² elements
- number of additions: N²
- \rightarrow operations-transfer ratio = 1/3 or O(1)

Device Transfer Costs

Transferring the data to the device is also important

- computational benefit of a transfer plays a large role
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Adding two (*N*×*N*) matrices:

- transfer back and from device: 3 N² elements
- number of additions: N²
- \rightarrow operations-transfer ratio = 1/3 or O(1)

Multiplying two ($N \times N$) matrices:

- transfer back and from device: 3 N² elements
- number of multiplications and additions: N³
- \rightarrow operations-transfer ratio = O(N) grows with N

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Programming Strategy

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Use GPU to complement CPU execution

- recognize parallel program segments and only parallelize these
- · leave the sequential (serial) portions on the CPU

parallel portions (enjoy)

sequential portions (do not bite)



PPP (Peach of Parallel Programming - Kirk/Hwu)

Course Schedule

Introduction (KM)

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1:30 - 1:45:

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5:25 – 5:30:	Closing remarks (KM, FX)	
4:45 – 5:25:	CT reconstruction examples (FX, KM)	
4:30 – 4:45:	CUDA programming environment (FX)	
3:45 – 4:30:	CUDA API, threads, memory, performance optimization (KM	I)
3:30 – 3:45:	GPU hardware (KM)	
	Coffee Break	
2:30 – 3:00:	Parallelism in CT reconstruction (FX)	
2:15 – 2:30:	Parallel programming primer (KM)	
1:45 – 2:15:	Introductory code examples (KM)	
1.50 1.45.		