5 → Tw
5 → lw
3 → beq
4 → add
4 → sw

# not taken

How many clk cycles does it take to execute?

\[ 800 \times 5 = 4000 \text{ ns} \]

- Single cycle
- Multi cycle
- 24 clk cycles

= 2100 ns
SW

7-opcode function

Fetch
Decide
Addr Calc
Save to Mem
gate logic for control

Next State

Any opcode

Any state
Microprogramming

Seg of each instr type

lw: Fetch
    Decode
    AW Addr
    Mem
    WB to Reg

Write RegWrite
Single cycle

lw 200ns
sw 175ns
lhrs 100ns
def 70ns
f 70ns

Map -> [0] crnt_paths

length clock cycle

multicycle

map bubble -> length clock cycle

max bubble for code
addi $t0, $t1, 8

Reg[r+1] = Reg[rs] + 8
A

ALU00t = Reg[rs] + 8
= A + 8
jr $ra + PC = Reg[rs]
jr $ra + PC = Reg[rs]