Excited for Every Instruction
Stage 1: Decode or Control

A = Reg[rs] + 4
B = Reg[rt] + 4

Decode opcode/func

ALUOut = PC + 4 + (st imm red <c2>)

Executed for all instructions
Stage 2:

Stage 3: Mem Read

Stage 4: Write Back

M\text{DR}[r+1] = M\text{DR}

M\text{DR}[r+0] = \text{Mem}[\text{ALUOut}]

\text{ALUOut} = \text{Reg}[r3] + \text{SB imm red}

\text{Data}_{\text{MDR}} = \text{Instr}_{\text{Data}}
Stage B: Store to mem

\[ \text{Mem}[\text{AWOut}] = B \]
Stage 6: ALUOut = A op B

Stage 7: Reg[rd] = ALUOut
Stage 3:
PC = PC + 4 + (SE | imm << 2)
j

Fetch

Decode

PC = PC + 4 \times [31:26] \text{ IR}[25:0] \ll 2