\[ C_{0,0} = A + B \]
\[ C_{1,0} = A' + B' \]
\[ C_{2,0} = (AB)' \]
\[ C_{2,1} = A'B' \]
\[ C_{2,0} + C_{1,0} = C_{2,0} + C_{1,0} \]

\[ \text{LSB} \ C_{im} = C_1 \]
<table>
<thead>
<tr>
<th>C2C1C0</th>
<th>(A \oplus B)</th>
<th>A NAND B</th>
<th>A AND B</th>
<th>A - B</th>
<th>A OR B</th>
<th>A' OR B'</th>
<th>8-LT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Diagram:

- A and B are inputs to an XOR gate.
- The output of the XOR gate feeds into a D flip-flop.
- The flip-flop has a carry input (Cin) and outputs (A', B', Cout).
- The flip-flop's outputs are connected to a counter labeled 6 1 2 3 4 5 6 7 8-LT.
\[
\begin{array}{c|c|c}
A & B & A \oplus B \\
\hline
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

\[
\begin{array}{c|c|c}
A \oplus B & C_{in} & (A \oplus B) \oplus C_{in} \\
\hline
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]